OpenVVVF

INDEX

Testing and Validation

> Formal test reports and validation evidence for OpenVVVF hardware, firmware, and integration.

1. Testing and Validation

This section contains formal test records and validation evidence. Each document is evidence that a specific feature, requirement, or hazard mitigation was exercised.

1.1. Test evidence dashboard

1.1.1. Hardware

Test ID	Name	Motor class	Status	Trac
1	PMSM Resistance Calibration Validation	PMSM	draft	moto
2	PMSM Inductance Calibration Validation	PMSM	draft	moto
3	Power Resistor Sanity Check	-	draft	moto
4	Induction Motor Testbed	Induction	draft	moto
5	Induction Motor Resistance Calibration Validation	Induction	draft	moto
6	Inductance Calibration Validation	Induction	draft	moto
7	Induction Motor 1-Hour No-Load Test	Induction	draft	gate-
8	Induction Motor 180 V Power Stage Bring-up	Induction	draft	powe
9	Induction Motor 180 V 20-Minute Reversal Test	Induction	draft	direc
10	Motor Self-Commissioning Accuracy Report	PMSM + Induction	draft	moto

These reports validate the calibration routines on the C2 test fixture. The same routines are used on all OpenVVVF chassis; add a new report only when a different motor or harness is introduced.

1.1.2. Safety-mechanism validation

Test ID	Name	Scope
-	Fault-Injection Test Plan	component / system / integration / environmental fault injection (c

The fault-injection plan spans all test domains, so it is filed directly under Testing. Execution campaigns produce dated test reports filed as siblings of the plan, referencing it by test ID.

1.2. Domains

Documents are filed by **what is being tested**, not by what equipment the bench uses:

- **Hardware** - The DUT is physical hardware: power-stage bring-up, thermal, and bench characterization. Firmware-routine validations whose error budget is power-stage physics (e.g. motor self-commissioning calibrated against instruments) also live here.
- **Firmware** - The DUT is control-module firmware logic: unit tests and host- or bench-based tests that do not inject physical faults.
- **Integration** - System-level tests combining control module and power stage.